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COMPENSATION OF CURRENT TRANSFORMERS BY MEANS OF FIELD PROGRAMMABLE GATE ARRAY

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Abstract

With the diffusion of non-linear and unbalanced loads, which often cause unacceptable quality level of energy, energy quality monitoring represents an increasing need. Analyzing conducted disturbances requires measuring instrumentation, and thus voltage and current transducers, with large bandwidth. Voltage and current transformers (CT) are the most often installed transducers in electrical power system and typically they are constructed to operate at industrial frequency 50/60 Hz, but it is clear that their substitution would require an unsustainable cost. Therefore in this paper a digital technique for the compensation of CT, based on field programmable gate array, is presented: it implements a digital filter with a frequency response equal to the inverse one of the CT. The compensated CT continues to be an analog device since the FPGA board is opportunely equipped with analog-to-digital and digital- to-analog converters.

Keywords: current transformer, compensation, digital filter, optimization, power quality.

1. Introduction

The growing number of non-linear and unbalanced loads in the electrical systems increases the scientific interest in harmonic and inter-harmonic analysis. Nevertheless, the standards related to the type tests for accuracy of measuring instrument transformers [1], [2] which now are the only ones to account when calibrating voltage or current transducers, establish the way to test the accuracy only at the rated frequency and amplitude, and they do not say anything about how to find the frequency response and the linearity of such instruments. This, on the other hand, is in contrast with other standards related to power quality phenomena [3], [4], in which requirements for harmonic measurement are established: a power quality instrument must have the capability to measure spectral components of the grid voltage at least up to the 40th harmonic frequency. Of course, since the harmonic components have the amplitude and frequency different from the fundamental one, the accuracy of power quality instruments, and thus of instrument transformers, has to be determined also in these situations.

Voltage and current transformers (VT and CT) are the most often installed transducers in electrical power systems and typically they are constructed to operate at industrial frequency, 50/60 Hz. It is clear that their substitution would require an unsustainable cost, even if justified by the growing cost linked to bad power quality firstly coming, in turn, from the lack of energy quality monitoring. Therefore, the use of low cost devices, with which increasing measuring transformers' accuracies, would be of great interest. In scientific literature several papers face the issue of compensating CT and VT [5]-[7]. They all present techniques for compensating measuring transformers only at industrial frequency. So, in this paper a technique for compensating current transformers in a wide frequency range, 10 Hz to 10 kHz, is presented. It is based on the identification of a digital filter implemented on an FPGA

board, provided in analog-to-digital (ADC) and digital-to-analog (DAC) converters.

In section 2 a compensation method is shown; since it utilizes data from calibration of the CT, section 3 focuses on the description of an automated test system for the characterization of the CT.

Then, section 4 presents experimental results related to optimization and compensation.

2. Compensation method

Far from power transformers, current transformers can be considered as linear devices basing on some considerations. In fact, nonlinearity is almost completely due to one phenomenon, which is the magnetic core saturation [8]: it is directly proportional to the primary r.m.s. current and it is minimized by large turns ratio, small burden, small remanence flux, large core area and small secondary resistance. In general, current transformers are constructed in order to meet the last three requirements; regarding the burden, it has to be chosen according to the maximum power transferable from primary to secondary in order to maintain accuracy class. Finally, for what concerns primary r.m.s current., according to [2] the accuracy class has to be maintained in the range of 5 to 120 % of the primary current: of course its r.m.s. value depends on the amplitudes of fundamental and other frequency components. Anyway, since the contribution of a frequency component to the core magnetic flux is inversely proportional to its frequency [8] and, in most cases, their amplitudes are much smaller than the fundamental one, they can be surely neglected. Therefore, under the assumption that the primary current does not exceed 120 % of its rated value, a CT can be considered a linear device, as it is considered in most scientific papers proposing compensation techniques [5]-[7].

All the cited techniques, even if they reach considerable performance improvement factors in both ratio and phase errors, they do not consider the possibility of improving CT performance in a wider frequency range.

As a matter of fact, for a linear system the frequency response can be defined and thus another linear system with a frequency response equal to its inverse can be found: it is called its inverse linear system. Such a statement is the basis of the proposed compensation technique: once the CT has been metrologically characterized and its frequency response found, cascading a device with a frequency response equal to CT's inverse one, the performance will be improved in a wide frequency range.

3. Compensation of frequency response

A CT is a current transducer; in scientific literature, different proposals for compensating the frequency response of transducers [9]-[11] and of data acquisition systems [12]-[14] can be found. Some of them perform the compensation in the frequency domain, obtaining good results but with high computational effort that is not compatible with the proposed application. Some others perform the compensation in the time domain by a digital filter. Let us consider a transducer with a low linearity error. Under this assumption, it can be considered as a linear system and its frequency response is given by (1)

$$Y(f) = \frac{1}{R(f)e^{-i\varphi(f)}} X(f) \quad , \tag{1}$$

where X is and Y are the spectra of the signals before and after transduction, respectively, and f is the considered frequency. $R(f)$ and $\varphi(f)$ are the systematic modifications introduced by the transducer in amplitude and in phase, respectively, on the spectral component at frequency f

of the input signal. These systematic effects can be compensated by introducing a filter whose frequency response, $H_d(f)$, is exactly given by

$$H_d(f) = R(f)e^{-j\varphi(f)} = \frac{X(f)}{Y(f)}, \tag{2}$$

for any frequency in the range of interest. The H_d function can be obtained performing a proper transducer characterization.

The analog implementation of transfer function (2) is obviously not easily practicable and it can lead to acceptable results only if applied to a very limited frequency range. Better results can be obtained with digital filtering.

Two main implementations for digital filters exist: FIR and IIR. FIR filters are relatively simple to compute, inherently stable but their main drawback with respect to IIR filters is that they may need a large number of coefficients to approximate the desired response. This makes them ineffective for the aim of this paper. An IIR filter is generally modeled by a transfer function in the z domain that can be written as

$$H(z) = \frac{b_0 + b_1 z^{-1} + ... + b_m z^{-m}}{1 + a_1 z^{-1} + ... + a_n z^{-n}}, \tag{3}$$

With this approach, filter design requires the choice of best values for parameters a_1, …, a_n *and* b_0, b_1, …, b_m so that its transfer function approximates the desired frequency characteristic. In addition, m and n, the order of the numerator and the denominator, respectively, are design parameters that should be chosen too. The problem is that unlike the FIR filters, there is no standard design approach for obtaining optimal approximations of an arbitrary frequency response with IIR filters.

The choice of the best coefficients for optimal approximation can be formulated, from the mathematical point of view, as an inverse problem [15] and solved by adopting optimization techniques [16]. An objective function, describing the difference between desired and obtained frequency responses has to be defined and minimized by an optimization algorithm. The choice of the chosen objective function at the same time affects the optimality of the solution and the computational complexity of the research. Minimization, performed with deterministic algorithms, is very sensitive to the initial point[15], [16][16],and the obtained filters, in some cases, have an unacceptable complexity to perform on-line compensation. In other cases, the compensation does not reduce the uncertainty below 0.1 %. More effective methods, such as hybrid optimization techniques [17]-[19] are never applied to such a task. Therefore, in the following, such a procedure is described and applied for designing a digital filter that performs compensation of the frequency response of a CT.

4. Identification procedure

The optimization problem studied here has a nonlinear objective function with $n+m+1$ independent variables. Therefore, the research space should be $\Re^{n+m+1}$, where $\Re$ is the whole set of real numbers. Nevertheless, this interval can be reduced by adopting, as commonly done in a wide class of optimization problems, some constraints on solution characteristics. The constraints divide the search space into feasible and infeasible regions with remarkable reduction of the computational burden. Constraints can be of two types:

- equality and inequality constraints;
- bounds on variable values.

A solution that does not satisfy all the constraints and all the bounds is called infeasible solution, and it is ignored. In the considered problem, a constraint comes from the requirement of filter stability: the poles of the digital filter must have a modulus less than one, so a nonlinear inequality constraint is imposed. Moreover, to obtain solutions that can be easily implemented by adopting fixed-point arithmetic, bounds on variable values have been set to -1 and 1, so obtaining normalized coefficients. These conditions restrict the research space to the interval $(-1,1)^{n+m+1}$, with a remarkable reduction in computational burden without loss of generality.

An objective function for the considered problem has to take into account the improvements that are obtained with the introduction of the filter, in terms of reduction of ratio errors and phase displacements. To evaluate these reductions in the whole input frequency range, an extension of definitions reported in international standards [2] with reference to the fundamental frequency have been adopted [11],[20]. In fact, the obtained reductions can be evaluated at different frequency N_f in the range of interest and then, these values can be combined to express the global reduction. The ratio error and phase displacement can be calculated before filter introduction with (4) and (5), respectively, for each of the frequencies, f_k. Then, the same indexes can be calculated after filter introduction with (6) and (7), where $H(f)$ is the frequency response of the implemented filter. The objective function proposed in order to combine all these values is reported in (8). It is composed of two terms that are, respectively, the mean quadratic values of relative improvements of ratio error and phase displacement. With an ideal filter compensation, $H(f)$ is equal to $H_d(f)$ in (2), and so ΔR_C and $\Delta\varphi_C$ are zero and thus F reaches its minimum value that is zero too. In practice, the smaller the objective function value the better is the compensation done by the filter. The objective function should be minimized by searching for best filter coefficients that produce a transfer function, minimizing, in turns, the ratio errors and phase displacements.

$$\Delta R(f_k) = 100\left(\frac{1}{R(f_k)} - 1\right), \tag{4}$$

$$\Delta\varphi(f_k) = \varphi(f_k), \tag{5}$$

$$\Delta R_C(f_k) = 100\left(\frac{|H(f_k)|}{R(f_k)} - 1\right), \tag{6}$$

$$\Delta\varphi_C(f_k) = arg\,H(f_k) - \varphi(f_k), \tag{7}$$

$$F = \frac{1}{2}\left(\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\frac{\Delta R_C(f_k)}{\Delta R(f_k)}\right)^2} + \sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\frac{\Delta\varphi_C(f_k)}{\Delta\varphi(f_k)}\right)^2}\right). \tag{8}$$

Numerical research of the minimum in the objective function is performed with a hybrid technique based on the combination of a stochastic [18] and deterministic [19] approach. The two approaches are adopted in a combined way to take advantage of their complementary characteristics. In fact, the deterministic approach is fast to converge to a solution, but the quality of results strongly depends on the choice of the starting point. Non-deterministic approaches do not depend on the initial choice but usually are slow to find the optimal

solution. Starting from these considerations, an initial exploration of the space of solutions is made by a generic algorithm having a population size greater than the number of coefficients chosen as the target. Then, the obtained values have been used as initial points to run a constrained deterministic approach based on the Sequential Quadratic Programming (SQP) [19] to find the optimal solution. The SQP algorithm was preferred to simpler algorithms (such as the zero-order method) for the possibility to take into account the information about the derivative of the objective function and, in addition, to include, in direct way, the above-mentioned constraints [19].

The described procedure has three parameters that can be chosen arbitrarily: the sampling frequency and the number of coefficients of the filter numerator and denominator. The sampling frequency should be chosen according to the target application. For the case in hand, as it will be seen in the next subsection, since the digital filter has to be implemented on the FPGA board with 200 kHz ADC and DAC, the sampling frequency is chosen equal to 200 kHz. The lengths of the numerator and denominator should be fixed very carefully because they involve, at the same time, the number of independent variables of the objective function and the complexity of the obtained filter. Typically, better results are obtained increasing the filter order, but this is against the need of keeping the filter computational burden low. For this reason, the procedure is repeated a certain number of times, varying in each run the numerator and denominator lengths to find their best values. The lengths of the denominator, n, and of the numerator, m+1, are chosen in the range of 5÷12 and the population size of the generic algorithm 50 greater than the n+m+1 value, *i.e.* the number of independent variables. The inner loop is repeated 3 times.

The identification procedure is made in this way: first of all, the transfer function defined in (1) is constructed in a numerical way, linearly interpolating experimental data from calibration. The optimization algorithm runs in three nested loops, varying the numerator and denominator lengths; in the inner loop the procedure is repeated a certain number of times. This is required, basing on the fact that the utilized hybrid optimization technique comprehends a stochastic algorithm which returns different results in every run. The number of frequency points is chosen equal to four times the total number of coefficients. Among the solutions referring to the same numerator and denominator lengths, which come from the inner loop, the one which minimizes the cost function is chosen.

5. Implementation on FPGA board

The identified digital filter represents the inverse linear system of the characterized CT. In order to real-time compensate the CT, a digital processor, opportunely equipped with analog-to-digital and digital-to-analog converters, has to be used. For the case in hand, an FPGA board has been used. It contains an ADC and a DAC with 16 bit resolution and 200 kHz maximum sampling frequency for the first one, 1 MHz for the second. The block scheme of the compensated CT is shown in Fig. 1.

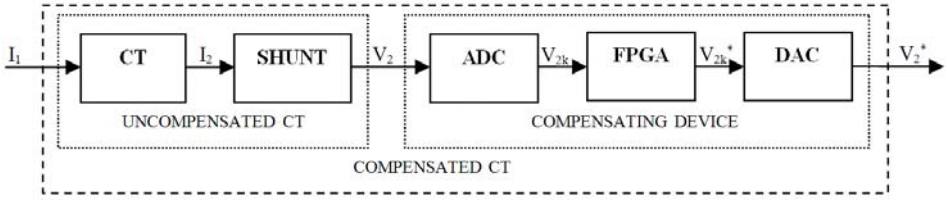

Fig. 1. Block scheme of the compensated current transformer.

In Fig. 4, I_1 is the primary current, I_2 the secondary current, V_2 the voltage across the shunt at the secondary winding, V_{2k} the sampled version of V_2, V_{2k}^* the filtered version of V_{2k}, V_2^* the analog version of V_{2k}^* and it is the output of the compensated CT. Such an instrument transformer continues to be an analog device, thus offering the possibility of being employed in whatever measuring system.

6. Current transformer metrological characterization

For the metrological characterization of current transformers an automated measuring station has been realized: it is based on a power source, numerically controlled, and a PXI platform. Its block scheme is shown in Fig. 2 and its features are described in [11] The outputs of the reference shunt and of the CT are simultaneously sampled and acquired through a data acquisition board and they are compared. The software for the automated measuring station has been implemented in LabWindows CVI, a C programming environment, measuring instruments oriented, distributed by National Instruments.

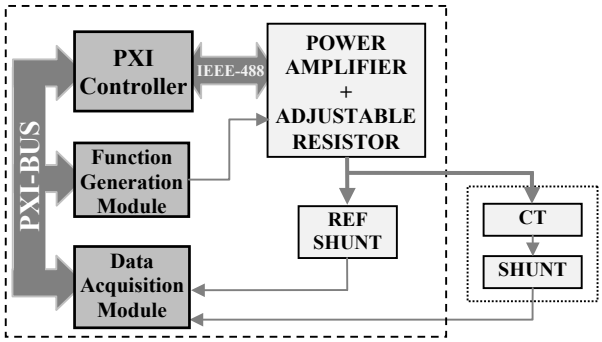

Fig. 2. Block scheme of the realized calibration station.

The measuring station is programmed in such a way that it automatically performs the desired number of tests in order to determine the mean transformation ratio, the frequency response and the linearity of the CT under test, as described in [11].

For the case in hand, a CT with ratio 150/5 A/A, accuracy class 0.5 and rated power of 5 VA has been utilized; using three primary supplementary turns its rated ratio becomes 50/5 A/A. A preliminary test in order to determine the ratio at rated frequency, 50 Hz, and rated current, 50 A, has been conducted: the ratio is 10.01 A/A. The CT has been characterized in the frequency range of 20-10000 Hz at rated current of 50 A, using a resistive shunt of 100 mΩ at the secondary winding. According to [1], [2] the ratio error and phase displacement of the CT are found and they are shown in Fig. 3: it is evident that the ratio error is equal to zero at 50 Hz.

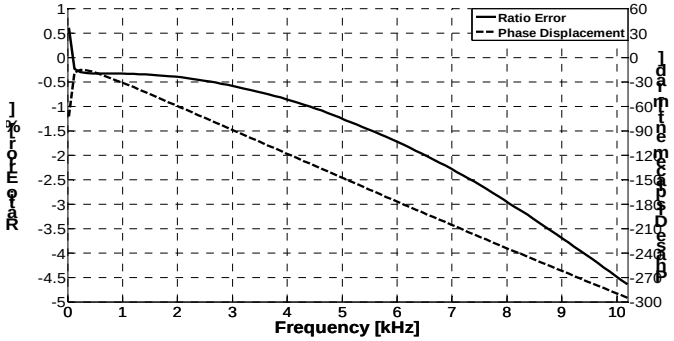

Fig. 3. Ratio error and phase displacement of current transformer.

7. Experimental results

Data available from calibration of the CT are used in an optimization procedure, in order to find the digital filter that minimizes the ratio error and phase displacement of the compensated CT. This digital filter is then implemented in the FPGA compensating device and the compensated CT is characterized with previously described automated measurement station. Optimization and compensation results are discussed in the next subsections.

7.1. Optimization results

The procedure described in section 2A has been used in order to identify a digital compensating filter for the utilized CT, whose metrological characterization is described in section 3. As previously said, the sampling frequency of the digital filter is chosen equal to 200 kHz, since it is the sampling rate of A/D and D/A converters on the FPGA board. Denominator and numerator lengths, n and m, are chosen in the range of 5÷12 and population size of genetic algorithm 50 greater than the $n+m$ value. The inner loop is repeated 3 times. To compare the improvements introduced by the different solutions, two indices have been used, as in formulas (7) and (8), where I_R and I_φ are, respectively, improvements in ratio error and phase displacement. In Figs 4 and 5, I_R and I_φ for CT as functions of numerator and denominator lengths are shown. The best digital compensating filter, which minimizes the objective function, has 11 zeros and 11 poles; numerator and denominator coefficients are shown in Table 1. Improvements in ratio error and phase displacement, coming from simulations for the adopted solution, are respectively equal to 24.4 and 22.8.

$$I_R = \frac{\overline{\Delta R^2}}{\overline{\Delta R_C^2}} = \frac{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\Delta R(f_k)\right)^2}}{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\Delta R_C(f_k)\right)^2}} \tag{9}$$

$$I_\varphi = \frac{\overline{\varphi^2}}{\overline{\varphi_C^2}} = \frac{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\varphi(f_k)\right)^2}}{\sqrt{\frac{1}{N_f}\sum_{k=1}^{N_f}\left(\varphi_C(f_k)\right)^2}} \tag{10}$$

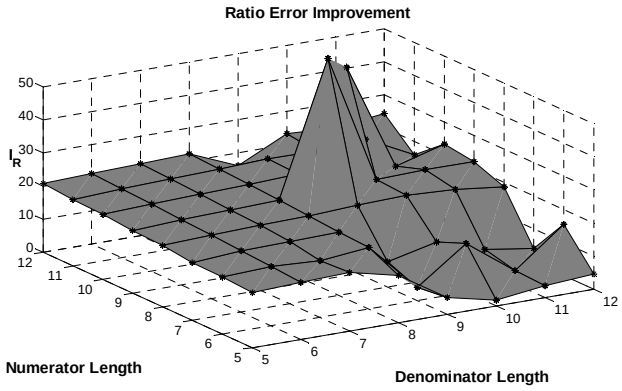

Fig. 4. Improvement of ratio error as function of numerator and denominator lengths.

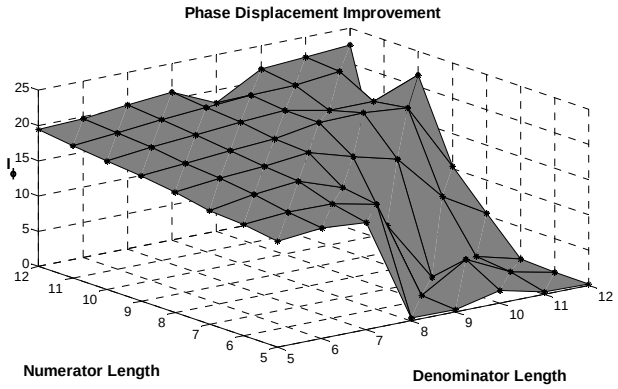

Fig. 5. Improvement of phase displacement as function of numerator and denominator lengths.

7.2. Compensation results

The identified digital filter, whose coefficients are shown in Table 1, has been implemented in the FPGA board and the compensated CT has been characterized through the previously described automated measuring station. The same tests reported in section 3 have been performed.

Table 1. Coefficients of compensating digital filter.

b_k	a_k
1.747893	1.000000
0.544851	-0.010405
-0.162473	1.006314
0.000000	0.000017
-0.002149	0.446846
0.510690	-0.012168
0.805931	0.575127
0.358222	0.034914
0.265825	0.750312
0.101732	0.030656
-0.055858	0.279981
0.134157	0.137621

Ratio error and phase displacement of the compensated CT are shown in Fig. 6. It can be seen that the phase displacement of the compensated CT is worse than that of the uncompensated one: this is due to the fact that the compensating device introduces a time delay related to A/D conversion, filtering and D/A conversion, and it adds a phase displacement, a linear function of frequency, to the output of the compensated CT. The total time delay has been measured and it is equal to 10.55 μs. Obviously, since it is constant, it can be eliminated in post-processing.

In Table 2 the mean quadratic values for ratio errors and phase displacements of uncompensated and compensated CTs and compensation improvements are reported. In it, *S* refers to simulation values, *M* to measurement values, *IS* is the improvement in simulation, *IM* the improvement in measurement, *IMpp* the improvement in measurement with data post-processing. Improvement in ratio error is approximately the same, both in simulation and measurement. As it is said before, the phase displacement is worse due to the time delay of the compensating device; if the output of compensated CT is post-processed, the improvement both in simulation and measurement is approximately the same.

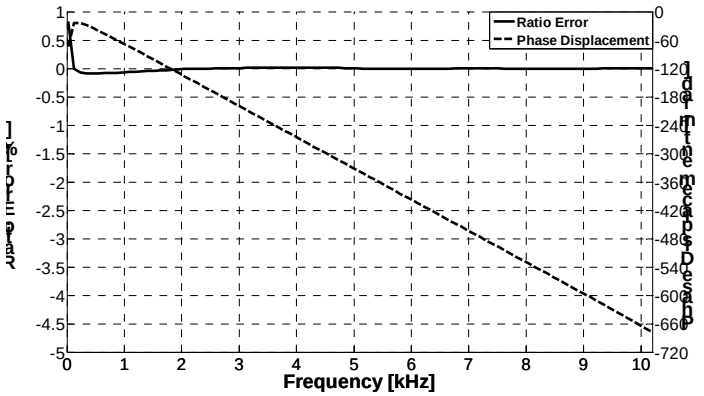

Fig. 6. Ratio error and phase displacement of compensated CT.

Table 2. Compensation improvements in ratio error and phase displacement.

	Ratio error				Phase displacement				
	S [%]	*M* [%]	*IS* [p.u.]	*IM* [p.u.]	*S* [mrad]	*M* [mrad]	*IS* [p.u.]	*IM* [p.u.]	IM_{PP} [p.u.]
CT	2.17	2.17	24.4	24.1	173.1	173	22.8	0.44	22.7
Comp. CT	0.089	0.090			7.6	391.6			

8. Conclusions

In this paper a real-time digital technique for the compensation of current transformers in the frequency range of 10 Hz – 10 kHz, based on a field programmable gate array, has been presented. It is based on the identification of a digital filter with a frequency response equal to the inverse one of the CT. Once the CT has been metrologically characterized, thus finding its frequency response, filter coefficients are found through the optimization procedure; the compensated CT continues to be an analog device since it is obtained by cascading the CT with an FPGA board, opportunely equipped with analog to digital and digital to analog converters, which implements the digital filter. Experimental results have shown that the compensated CT improves the performance of the original CT; the ratio error steps up by a factor of 24.1.

Regarding the phase displacement, it grows worse due to the presence of a time delay introduced by the compensating device: since this time delay is constant, it can be eliminated by post-processing of the output of the compensated CT, reaching in this way an improvement factor of 22.7 also in phase displacement.

The presented technique, other than improving CT performances in a large frequency bandwidth, is effective also from another point of view: the improvement is obtained adding to the CT a low cost device, increasing a little the total CT cost. A CT with the same performance of the compensated CT has a cost higher than the original one by about the improvement factor obtained with the compensation.

Future work will regard the enhancement of mathematical formulation of the identification procedure, in order to account for the phase displacement due to the time delay of the compensating device, and the use of such a technique for active compensation of CTs.

References

[1] "IEEE Standard Requirements for Instrument Transformers", IEEE Std. C57.13-1993, 1994.

[2] “Instrument Transformers-Part 1: Current Transformers”, IEC Std. 60044-1, 2000.
[3] EN 50160, “Voltage characteristics of electricity supplied by public distribution systems”, CENELEC, 1999.
[4] IEC EN 61000-4-30: “Testing and measurement techniques – Power quality measurement methods”, 11/2003.
[5] P. Daponte: “Electronically compensated current transformer modeling”. *Measurement*, no.15 (4), 1995, pp. 213-222.
[6] A. Baccigalupi, A. Liccardo: “Compensation of Current Transformers”. *Instrumentation and Measurement Technology Conference Proceedings, 2007 IEEE,* 1-3 May 2007.
[7] D. Slomovitz: “Electronic system for increasing the accuracy of in-service instrument-current transformers”. *Instrumentation and Measurement, IEEE Transactions on*, vol. 52, no. 2, 2003, pp. 408 – 410.
[8] D. A. Douglass: “Current Transformer Accuracy with Asymmetric and High Frequency Fault Currents”. *IEEE Transactions on Power Apparatus and Systems,* vol. PAS-100, no. 3, 1981, pp. 1006 – 1012.
[9] C. De Capua, C. Landi: “Measurement Station Performance Optimization for Testing on High Efficiency Variable Speed Drives”. *IEEE Transactions On Instrumentation And Measurement*, vol. 48, no. 6, 1999, pp. 1149 – 1154.
[10] G. Dantona, A. Ferrero, R. Ottoboni: “Bandwidth enhancement of an insulated voltage to voltage transducer via digital compensation for industrial applications”. *Instrumentation and Measurement Technology Conference, 1998. IMTC/98. Conference Proceedings. IEEE,* vol. 1, 18-21 May 1998, pp. 380 – 384.
[11] A. Delle Femine, D. Gallo, C. Landi, M. Luiso: “A technique for real-time correction of measurement instrument transducers frequency responses”. *International Instrumentation and Measurement Technology Conference Proceedings*, *2008 IEEE*, May 12–15, 2008.
[12] R. Pintelon, Y. Rolain, M.V. Bossche, J. Schoukens: “Towards an ideal data acquisition channel”. Instrumentation and Measurement”. *IEEE Transactions on,* vol. 39, no.1, Feb 1990, pp. 116-120.
[13] I. Kollar, R. Pintelon, Y. Rolain, J. Schoukens: “Another step towards an ideal data acquisition channel”. *Instrumentation and Measurement, IEEE Transactions on*, vol.40, no. 3, June 1991, pp. 659-660.
[14] I. Kollar, Y. Rolain: “Complex correction of data acquisition channels using FIR equalizer filters”. *Instrumentation and Measurement, IEEE Transactions on,* vol. 42, no. 5, Oct. 1993, pp. 920 – 924.
[15] J. Kaipio, E. Somersalo: “Statistical and Computational Inverse Problems”. *Applied Mathematic Sciences,* 2005.
[16] K. Deb: Multi-Objective Optimization using Evolutionary Algorithms, Wiley, 2001.
[17] J.H. Holland: *Genetic algorithms* , Scientific American, 1992.
[18] D.E. Goldberg: Genetic Algorithms in Search, Optimization, and Machine Learning, Addison Wesley, 1989
[19] T.F. Coleman, Y. Li: “An Interior, Trust Region Approach for Nonlinear Minimization Subject to Bounds”. *SIAM Journal on Optimization*, vol.6, 1996, pp. 418-445.
[20] A. Delle Femine, C. Landi, M. Luiso: “A Fully Automated Measuring Station for the Calibration of Voltage Transducers”. *Proceedings of 15th IMEKO TC4 Symposium on Novelties in Electrical Measurements and Instrumentation*, 19-21 September 2007, Iasi, Romania.